WHAT IS CLAIMED IS:

1.

A processor comprising:

a clock signal generator generating clock signals;

an operational processing part performing data processing which is divided into a plurality of execution units, in accordance with the clock signals;

a storage storing data used when each execution unit is executed by the operational processing part;

a data amount detector detecting amounts of the data stored in the storage per each execution unit;

a clock frequency determining part determining a new clock frequency of the clock signals by using the amounts of the data, said clock signals being supplied newly to the operational processing part.

2.

A processor according to claim 1, wherein the execution units include a predetermined execution unit,

wherein the data amount detector detects per each predetermined execution unit.

3.

A processor according to claim 1 further comprising:

an input port receiving the data to be processed by the operational processing part,

wherein the data amount detector detects amount of the data received by the input port.

4.

A processor according to claim 1 further comprising:

an output port outputting the data obtained by performing the data processing,

wherein the data amount detector detects amount of the data output by the output port.

5.

A processor according to claim 1 further comprising:

an execution priority storage storing preliminary priorities which indicate the execution order of the execution units,

wherein the clock frequency determining part selects one or more of the execution units in order of the lower priority, and determines the new clock frequency of the clock signals by using the amounts of the data associated with the execution units selected by the clock frequency determining part.

6.

A processor according to claim 1, wherein the clock frequency determining part includes a table which indicates the relation between the amounts of the data detected by the data amount detector and the variation of the clock frequency, and determines the new clock frequency of the clock signals by referring to the table.

7.

A processor according to claim 1, wherein the clock frequency determining part includes:

a table indicating the relation between the amounts of the data detected by the data amount detector and the variation of the clock frequency,

a clock frequency holder holding the practical current clock frequency supplied to the operational processing part,

an adder adding to the current clock frequency the variation obtained from the table,

wherein the clock frequency determining part

determines newly the output value of the adder as the clock frequency of the clock signals.

8.

A processor according to claim 7 further comprising:

an execution status detector detecting whether a certain execution unit becomes the predetermined state or not;

a timer newly starting the clocking when the execution status detector detects that the execution unit has become the predetermined state;

a clock frequency changing part changing the clock frequency, the clock frequency changing part decreasing the absolute value of the variation according to the value of the timer;

wherein the adder adds to the current clock frequency the variation which is changed by the clock frequency changing part.

9.

A processor according to claim 1, wherein the storage includes a plurality of storage regions, each of which stores the data for each execution unit,

wherein the data amount detector detects the amounts of the data stored in each storage region,

wherein the clock frequency detecting part obtains a plurality of clock frequencies on the basis of the amounts of the data associated with each execution unit, and determines the highest clock frequency among said plurality of clock frequencies as the new clock frequency to be supplied newly to the operational processing part.

10.

A processor according to claim 9 further

comprising:

an input port receiving a data to be processed by the operational processing part,

wherein the clock frequency detecting part determines the new clock frequency on the basis of the amount of the data in the nearest storage region to the input port among said plurality of storage regions.

11.

A processor according to claim 9 further comprising:

an output port outputting a data after being processed by the operational processing part,

wherein the clock frequency detecting part determines the new clock frequency on the basis of the amount of the data in the nearest storage region to the output port among said plurality of storage regions.

12.

A processor according to claim 1, wherein the clock frequency detecting part includes a source voltage controller supplying a source voltage to the operational processing part, in accordance with the new clock frequency.

13.

A control device for a processor comprising:

a clock signal generator generating clock signals;

an operational processing part performing data processing which is divided into a plurality of execution units, in accordance with the clock signals;

a storage storing the data used when each execution unit is executed by the operational processing part;

a data amount detector detecting amounts of data in the storage;

a clock frequency determining part determining a

new clock frequency of the clock signals by using the amounts of data, said clock signals being supplied newly to the operational processing part.

14.

A clock frequency determining method determining a clock frequency supplied to a processor, which comprises an operational processing part processing data in accordance with clock signals and a storage storing the data used when each execution unit is executed by the operational processing part, comprising:

detecting amounts of data associated with the respective execution units, said data being stored in the storage;

determining a new clock frequency to be supplied to the operational processing part on the basis of the result of the detection;

generating clock signals supplied to the operational processing part in accordance with a new clock frequency.

15.

A source voltage controlling method, in which the source voltage is supplied to a processor comprising an operational processing part processing data in accordance with clock signals and a storage storing the data used when each execution unit is executed by the operational processing part, comprising:

detecting amounts of data associated with the respective execution units, said data being stored in the storage;

determining a new clock frequency to be supplied to the operational processing part on the basis of the result of the detection;

controlling the source voltage to be supplied to the operational processing part, following to the new

clock frequency.